JC19 Rec'd PCT/PTO 23 APR 2001

FORM PTO-1390 (REV 11-2000) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEYS DOCKET NUMBER 740119-124
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U S APPLICATION NO (If known, see 37 CFR 1 5) 09/830163
INTERNATIONAL APPLICATION NO. PCT/DK99/00579	INTERNATIONAL FILING DATE 22 OCTOBER 1999 (22.10.1999)	PRIORITY DATE CLAIMED 23 OCTOBER 1998 (23.10.1998)
TITLE OF INVENTION A VIDEO OUTPUT AMPLIFIER		
APPLICANT(S) FOR DO/EO/US Erik Albert JENSEN		

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. ☐ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☒ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information: Application Data Sheet and Five Sheets of Drawings (Figs. 1-6)

U S APPLICATION NO (If known, see 37 C F R 1 50)	INTERNATIONAL APPLICATION NO	ATTORNEYS DOCKET NUMBER
09/830163	PCT/DK99/00579	740119-124

21. ☒ The following fees are submitted	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(a)(1) – (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**	860.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(3)) paid to USPTO **$710.00**		
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$N/A	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	5- 20 =	0	X **$18.00**	$0	
Independent claims	1- 3 =	0	X **$80.00**	$0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$270.00**	$0	
TOTAL OF ABOVE CALCULATIONS =				$860.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.				$N/A	
SUBTOTAL =				$860.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$N/A	
TOTAL NATIONAL FEE =				$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 40.00	
TOTAL FEES ENCLOSED =				$900.00	
				Amount to be refunded:	$
				Charged:	$

a. ☒ A check in the amount of $900.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 19-2380 in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-2380(0119-124). A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO

SIGNATURE

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NAME

27,997
REGISTRATION NUMBER

April 23, 2001

Attorney's Docket No. 740119-124

IN THE UNITED STATES DESIGNATED/ELECTED OFFICE

In re Patent Application of	)	
Erik Albert JENSEN .	)	Group Art Unit: Unknown
International Application No.: PCT/DK99/00579	)	Examiner: Unknown
International Filing Date: October 22, 1999	)	
For: A VIDEO OUTPUT AMPLIFIER	)	

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Preliminary to calculation of the filing fee and examination of this application, please amend the above-captioned application as follows:

IN THE CLAIMS:

5. (Amended) A video output amplifier according to claim 1, characterised in that a continuing series of fast and strong dynamic intensity variations activate dynamic control current limiting means for one or both output transistors (TR2, TR3).

REMARKS

The amendment to claim 5 is to amend the multiple dependency.

Also attached is an Abstract.

Respectfully submitted,

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Date: April 23, 2001

AMENDED CLAIM

5. (Amended) A video output amplifier according to [any of the above claims] claim 1, characterised in that a continuing series of fast and strong dynamic intensity variations activate dynamic control current limiting means for one or both output transistors (TR2, TR3).

Abstract

Output amplifiers for driving picture tubes need to provide a high slew rate, and traditional class-A amplifiers have a high quiescent power consumption because of the high supply voltage combined with the necessary high quiescent current. According to the invention, the quiescent current is constituted mainly of the DC feedback current in the output device (TR3), and its control electrode is driven by means of a transistor (TR1), whose base has a reference potential, and whose emitter receives the static component of the control signal for the picture tube. In one embodiment the quiescent power consumption is 10-15% of that a corresponding class-A amplifier, and the required cooling means may be considerably reduced.

PCT/DK99/00579

A video output amplifier.

Amended text 12 October 2000

The invention relates to a video output amplifier for conversion of an intensity signal, consisting of a static and a dynamic component, into a control voltage for an electron gun in a cathode ray tube, comprising a first voltage supply with a voltage commensurate with the operating characteristics of the cathode ray tube, an input terminal for the video signal and an output terminal for the control voltage, and a linear amplification stage for at least the static component of the video signal, consisting of a first transistor, a linear push-pull amplifier stage for the fast dynamic components of the video signal consisting of said first transistor and a second transistor, and a third transistor for elevating the static component of the video signal from a voltage level corresponding to the input to that of the first supply voltage, and a feedback resistor. It is a purpose of the invention to provide a video output amplifier of this type in which the power loss is reduced considerably in comparison to known constructions in order that particular cooling means, such as cooling fins, may be avoided.

Cathode ray tubes (CRTs) are in general use in television receivers as well as in monitors for computer installations or personal computers, and video output amplifiers are used for driving such CRTs. Video output amplifiers are known and in practice comprise an output stage, the output terminal of which delivers a control voltage which is intended to control an electron beam in a CRT by modulating a suitably high voltage on the cathode. The bandwidth of the output signal is up to 5 MHz in generally known circuits for television. Discussions regarding television in the present text may be directly transferred to monitors and other equipment with a cathode ray tube.

The control voltage may be divided into two components: a static or only slowly varying component which contains the momentarily static intensities and slower intensity variations, and a dynamic component which contains the fast intensity variations. The input signal to the video output amplifier is provided by a signal processing circuit with output voltages in the range from +1 V to +6 V, while the output signal from the video output amplifer correspondingly is in the range +150 V

to +50 V which means that a video output amplifier for use in connection with television must have a supply voltage in the range +200 V. The fastest intensity variations in the output signal are ca. 100 V and occur in the course of ca. 100 ns which that a video output amplifier must be capable of delivering fairly large capacitive currents to the stray capacitances which load the output terminal which in its turn requires the quiescent current in amplifiers with class A output stages to be comparatively high.

The power loss in a class-A output stage is high. The comparatively high quiescent current combined with the high supply voltage cause the total power loss in the output stage to be high, and it becomes necessary to utilise external cooling means, such as cooling fins. In case the bandwidth of the video signal increases to e.g. 10 MHz, which is necessary in flicker-free television, where the deflection frequency is doubled, the power loss is correspondingly increased in a class-A output stage, and it is hence still more desirable to reduce the quiescent current in the output stage. To this end one may use e.g. a class-B output stage where an improvement may be obtained. One measure of the improvement may be the degree of increase in the proportion between the bandwidth of the video signal and the power loss of the video output amplifier used, and in class-B there is in practice obtained a halving of the power loss for a given bandwidth. Another measure of the improvement may be expressed as the reduction of the area below a curve which represents power drained from the voltage supply during a prescribed time function for the driving.

Circuits for the control of a CRT have been described in a series of articles in the German monthly FUNKSCHAU under the general title "Schaltungen zur Ansteuerung der Farbbildröhre", Part 1 (No. 21, 1987, p. 60), Part 2 (No. 22, 1987, pp. 83-86), Part 3 (No. 23, 1987, pp. 53-56). The amplifiers described are linear class AB and class B amplfiers. However, the known class AB output stages still have to use a considerable quiescent current, which only reduces the power loss to 50% with respect to a corresponding class A stage. The known class B output stages need a clamp function (a high voltage pulse has to be provided) to maintain the bias voltage for the upper output transistor, and this complicates the circuit considerably.

In US-A-4,293,875 there is described a digital circuit using few components for the control of a CRT when supplied with graphic or dot-matrix signals. This circuit will not provide gray levels unless assisted by a complex modulator circuit and it cannot be feed-back controlled.

In certain and normally undesirable signal situations, such as noise from an empty television channel, the dynamically caused power losses in class-B may increase considerably, which together with the required increase in bandwidth cause even such solutions to require special cooling means. It is hence the purpose of the invention to provide an amplifier circuit which displays considerably reduced quiescent power losses in comparison to known constructions, in order that special cooling means may be avoided.

This is obtained in a particular manner according to the invention as described in the characterising part of claim 1. Thereby it is in particular obtained that the power loss is reduced because a part of the quiescent current is constituted by the current which must run anyway in the feedback resistor. The expression "essentially directly" is to be understood such that there may be one or more circuit elements provided between the emitter and the source for supply voltage, e.g. for linearisation or frequency compensation. Furthermore the invention may be realised by means of any amplifying element which is suitable for the particular frequency range, such as an FET, a MOSFET or similar, where "base" is in general to be understood as "control electrode".

An advantageous embodiment is particular in that the base of the output transistor is driven via the collector of a further transistor, the base of which is connected to reference voltage at a low voltage level, and the emitter of which is supplied with the static component of the control signal as a current from a driver amplifier. Hereby it is obtained that the control signal for the static component is lifted to the correct base bias voltage for the output transistor. The dynamic component is predominantly supplied via a coupling capacitor.

A further particular embodiment is characterised in that the operating point for the further transistor is adjusted so that further to the static component it additionally

supplies rectified dynamic components to the base of the output transistor for the control of its dynamic output current for charging any stray capacitances present. Thereby it is obtained that the rectified dynamic components which would otherwise have been supplied via C4 do not cause a reversal of the charge of C4 which would otherwise manifest itself as long streaks following image sequences with many fast contrast jumps.

A further particular embodiment is characterised in that a second output transistor is driven in such a way that the discharge current is drawn out of stray capacitances present during negative jumps in the dynamic signal component. The second output transistor is biased such that it does not draw any appreciable quiescent current.

In particular the large difference between peak power and quiescent power may necessitate the use of a power limiting circuit, because a video signal which contains many contrast jumps, such as white noise on the input terminal, would be able to overload a circuit which due to the large power savings according to the invention has been made less bulky and with weaker cooling means. Ordinary signals would not be influenced by such a power limiting circuit. Hence a further embodiment is particular by the characteristics given in claim 5.

The invention will be described in greater detail in the following with reference to the drawing, in which

Fig. 1 is a schematic block diagram for video circuits comprising an output amplifier with a high supply voltage according to prior art,

Fig. 2 shows an embodiment according to the invention,

Fig. 3 shows an embodiment with a changed driver stage and an output buffer stage,

Fig. 4 shows a test signal which has been used to determine the power consumption in different amplifier constructions,

Fig. 5 shows the modelling of the power consumption from the voltage supply to a known construction based on a class-A amplifier, and

Fig. 6 shows the modelling of the power consumption for a construction according to the invention.

In Fig. 1 is shown a block diagram for a part of a television receiver or video monitor. In block 1 those signals are processed which are to drive the individual electron guns in a CRT. There are three output terminals corresponding to the three colours of phosphor which are to be activated, and each output terminal is controlled as to instantaneous light intensity. We are dealing with a signal which gives extremely fast transients with respect to slowly varying base levels, as one particular dot of phosphor on the screen may be totally black while its neighbour on the same line may have full intensity.

Amplification of the signals for use at the CRT in block 3 occurs in three identical video output amplifiers 2 to the colours R, G, and B. In the present embodiment for the prior art the CRT is driven at the cathode, but with suitable bias voltages and a phase reversal of the output signal it can equally be a control grid which is driven. Here only the conditions pertaining to the colour G will be described. The G signal from the circuit 1 is taken to the base of the driver transistor DTr which obtains its current from a low voltage supply. From the emitter an in-phase signal is taken to the output transistor TR which obtains it current supply from a relatively high voltage via a collector resistor Rc, corresponding to the requirements of the CRT. The local components required by a practical circuit for adjusting the operating point of the driver transistor are not shown. The operating range of the video output amplifier is in practice adjusted by an adjustment by means of an adjustment in the signal processing circuit in block 1, in the form a manual "cut-off" adjustment during manufacture or by means of a control loop so that it corresponds to the CRT used. In this construction both the DC or slowly varying component and the high frequency content are transferred. When the amplifier in the active range of the CRT must be both linear and have a large bandwidth, the transistor TR is driven in class-A. This causes a quiescent current which is large according to the circumstances, and in combination with the

high voltage droop across the output stage this causes a high quiescent power consumption - in practice for this type of output amplifier in the order of 2 W in case of typical television image information.

In Fig. 2 is seen an embodiment of the invention in the form of a G video output amplifier comprising the supply voltage indicated as 200 V, an input terminal and an output terminal for driving the CRT. The input signal is fed via a summing resistor R2 to the positive terminal of a voltage follower IC1, which i.a. provides a low impedance driver stage for the output transistor TR3 via the coupling capacitor C4. Simultaneously IC1 is also the driver stage for the dynamic component to TR2. IC1 receives its power from a low voltage supply which is not shown. The emitter of transistor TR3 is connected directly to the voltage supply, and the output voltage is taken from the collector. The same signal is taken to negative feed-back via the resistor R3 to the point of summation on the positive input terminal of the voltage follower IC1. From an AC point of view the supply voltage is at signal ground, and the transistor TR3 may hence dynamically be seen as a "grounded emitter". The transistor TR1 converts the output voltage from the driver stage IC1 into a control current which is taken to the base of transistor TR3. As the voltage on the output terminal of the voltage follower IC1 is largely identical to the voltage at the summation point on its input terminal, which contains the negatively fed-back signal, the operating point of TR1 may be adjusted by means of R8 and R10, so that the control current contains both the static control current and the rectified part of the dynamic control current required by TR3, whereby non-intended reversals of charge of C4 are avoided.

The output transistor TR3 delivers the required DC current to maintain the DC potential on the output terminal. Furthermore TR3 delivers the charging current to the stray capacitances (in the order of 15 pF) during positive voltage steps, because it draws the discharge current out of the stray capacitances. This construction has been used rather than a passive connection to ground, because the quiescent current may then be kept at a low value in the order of 1 mA, while the charge reversal current to the stray capacitances may reach 15 mA. TR2 is provided with a signal from the driver stage IC1 via the coupling capacitor C3. D1, R17 and R18 establish a

temperature compensated bias on the basis of TR2. The bias and R18 are determined so that the quiescent current in TR2 is maintained in the order of 1 mA mentioned and such that the bias on the base of TR2 may be influenced in the negative direction by the increasing control current which appears during many fast intensity variations. Thereby the control current to TR2 is limited and hence the dynamically determined power losses in order that no need for special cooling means arises. C3 is adjusted so that the time constant for the power limiting becomes large enough so that short series of fast intensity variations within a frame do not cause limiting. In practice the skilled person will fit linearising resistors in suitable places as well as current limiting resistors. Furthermore, a practical circuit would comprise a cut-off control loop, the function of which does not interfere with the present invention.

IC1 may advantageously be connected so that it provides a given voltage amplification, which gives a possibility of elevating the upper cut-off frequency of the video output amplifier.

In Fig. 3 is seen a video output amplifier according to the invention which is essentially identical in its function to that described with respect to Fig. 2. The difference is that the voltage follower IC1 is replaced by the emitter follower TR6 with the emitter resistance R4, and that there is added a buffer stage in the output consisting of the two transistors TR5 and TR4 with the zener diode D2. Furthermore there is shown a connection BCFB for beam current feedback.

In case the requirement for amplification and bandwidth is moderate it is sufficient to use an emitter follower TR6 as a driver. With an increase in the requirements it may be advantageous to use a discrete transistor amplifier with a certain voltage amplification as a driver in stead of the emitter follower TR6, and it may be further advantageous to comprise a limiter function in the transistor amplifer in such a way that the control current for TR3 is limited in the same way that the control current to TR2 is limited, cf. the description concerning Fig. 2.

It may be advantageous to include a buffer stage in the output of the amplifier, in particular if there is already a cut-off transistor, in that the dynamic power losses may

be distributed among four transistors rather than among only two. In the circuit of Fig. 3 TR4 functions as a cut-off transistor most of the time, where the slowly varying beam currents from the CRT are taken through TR4 to the video signal processing circuit via the terminal marked BCFB. During fast intensity variations TR4 functions as a buffer, because a part of the stray capacitances are discharged via TR4 and D2 to ground. The zener voltage on D2 is chosen such that the beam current is fed to the video signal processing circuit and not to ground. It is obvious that other voltage limiter circuits may perform the same function. TR5 is without current most of the time but it acts as a buffer during fast positive intensity variations where it charges a part of the stray capacitances.

In Fig. 4a is seen a test signal which is used in modelling a 5 MHz amplifier. The signal consists of two pulses with risetimes of ca. 100 ns, in that the pulses start from black and reach 50% and 100% maximum signal. The total duration of the test signal is ca. 3.5 µs, and it may be provided repetitively from a signal generator. The voltage amplitude on the input is 1 V and 2 V, respectively. The corresponding output signal is shown in Fig. 4b and goes from an output voltage of 160 V and falls during the two pulses to 110 V and 55 V, respectively. The signal is hence in reverse phase with respect to the input signal and is intended for cathode control of the CRT.

In Fig. 5 is shown the power consumption from the voltage supply of a 5 MHz output stage in class-A during the pulses, and it will be noted that the quiescent power is 1 W (black), and that the power consumption rises to 2 W (50% intensity) and 3.5 W (max. intensity) during the pulse cycle. As a measure of the power consumption it may be judged that the area below the curve is 6.5 µWs, i.e. the energy consumed during a pulse cycle. The power taken from the low voltage power supply is not taken into consideration.

In Fig. 6 is similarly shown the power consumption from the voltage supply of a 5 MHz output stage according to the invention. It is seen that the quiescent power consumption is ca. 0.25 W and that the power consumption is very low during the whole cycle, except where the output voltage (Fig. 4b) is intended to rise with a steep flank towards the quiescent value. Hereby power surges of 1.7 W and 3.2 W,

respectively, are obtained. These peaks are hence up to 12 times the quiescent power consumption. The area below the curve may be judged to be 0.3 μWs, i.e. an improvement of more than 20 times with respect to prior art expressed as a class-A stage. In a practical amplifier 8-10 times may be obtained. The power taken from the low voltage power supply is not taken into consideration in this case either.

Video output amplifiers according to the invention will be suitable for integration due to the small power consumption.

PATENT CLAIMS

1. A video output amplifier for conversion of an intensity signal, consisting of a static and a dynamic component, into a control voltage for an electron gun in a cathode ray tube, comprising a first voltage supply with a voltage commensurate with the operating characteristics of the cathode ray tube, an input terminal for the video signal and an output terminal for the control voltage, and a linear amplification stage for at least the static component of the video signal, consisting of a first transistor (TR3), a linear push-pull amplifier stage for the fast dynamic components of the video signal consisting of said first transistor (TR3) and a second transistor (TR2), and a third transistor (TR1) for elevating the static component of the video signal from a voltage level corresponding to the input to that of the first supply voltage, and a feedback resistor (R3), characterised in that the emitter of the first transistor is connected essentially directly to the first voltage supply, and that the base is driven by the static component of the video signal at a level adapted to the supply voltage, and in that the collector load for the static component of the video signal is essentially constituted by the feedback resistor (R3).

2. A video output amplifier according to claim 1, characterised in that the base of the third transistor (TR1) is connected to a reference voltage (Vref) at a low voltage level, and that the emitter of said third transistor is supplied with the static component of the control signal as a current from a driver amplifier (IC1, TR6).

3. A video output amplifier according to claim 2, characterised in that the operating point for the third transistor (TR1) is adjusted so that further to the static component it additionally supplies rectified dynamic components to the base of the output transistor (TR3) for the control of its dynamic output current for charging any stray capacitances present.

4. A video output amplifier according to claim 1, characterised in that the second output transistor (TR2) is driven in such a way that the discharge current is drawn out of stray capacitances present during negative jumps in the dynamic signal component.

5. A video output amplifier according to any of the above claims, characterised in that a continuing series of fast and strong dynamic intensity variations activate dynamic control current limiting means for one or both output transistors (TR2, TR3).

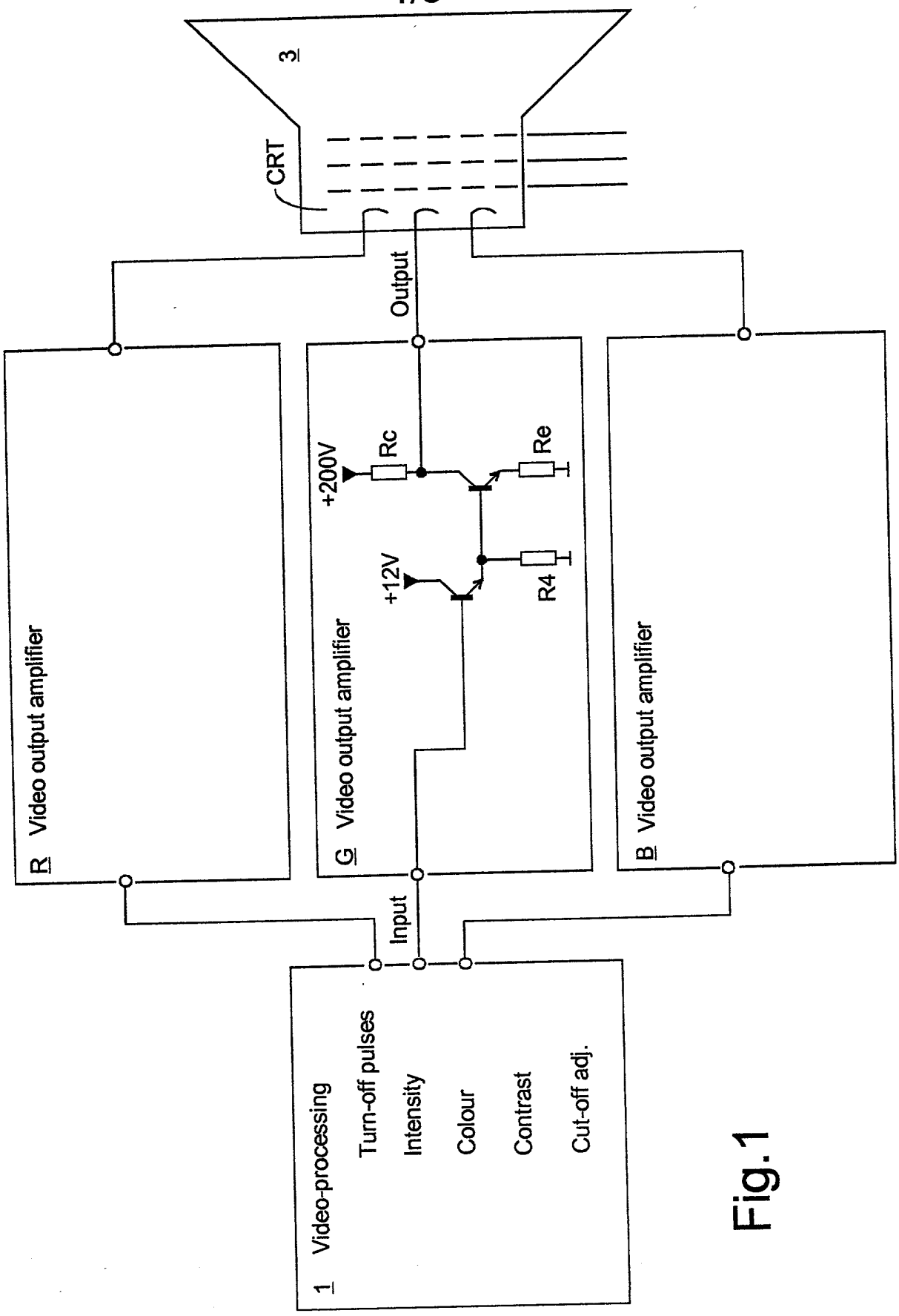
3
CRT
Output
R Video output amplifier
G Video output amplifier
B Video output amplifier
+200V
Rc
Re
+12V
R4
Input
1 Video-processing
Turn-off pulses
Intensity
Colour
Contrast
Cut-off adj.

Fig.1

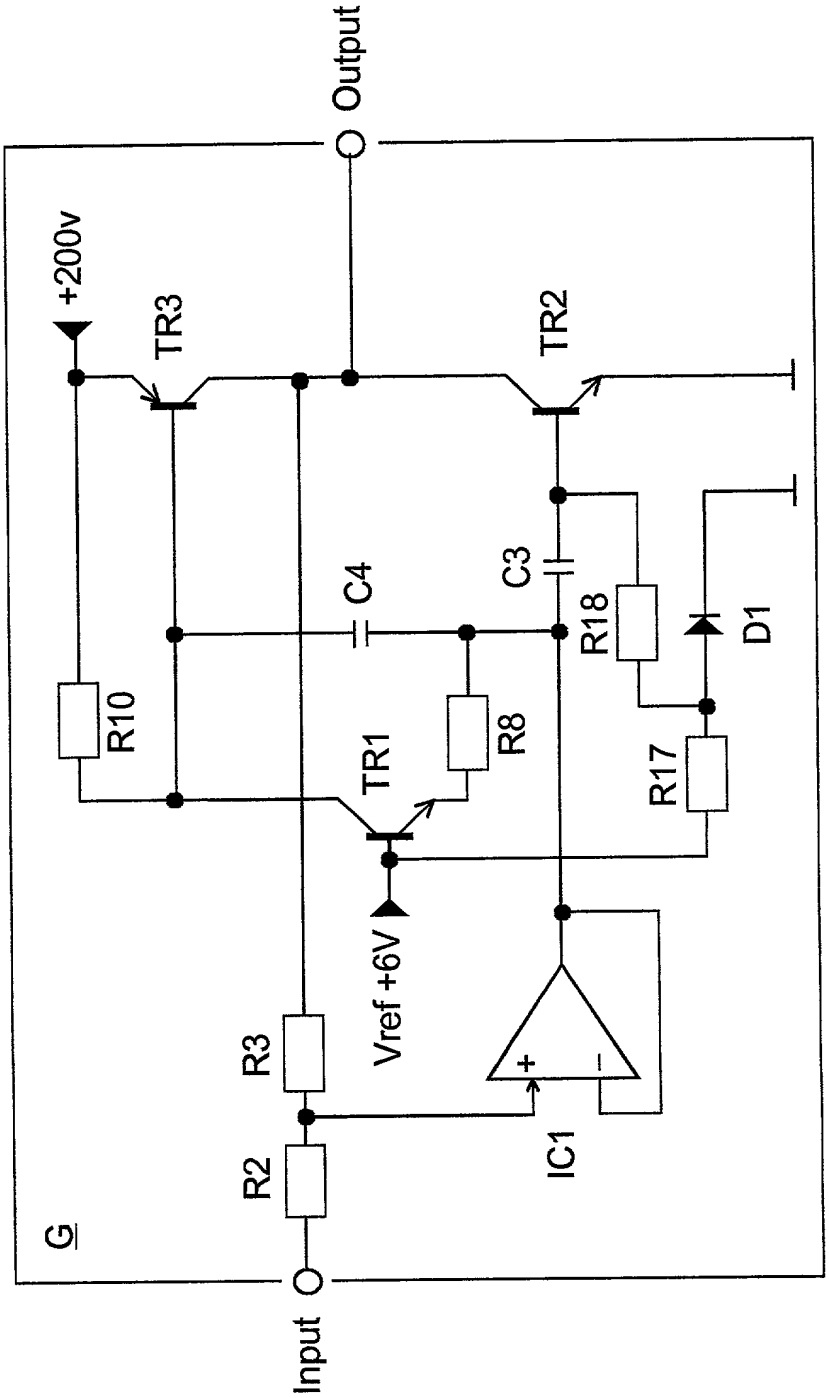
Output
+200v
TR3
TR2
C4
C3
R18
D1
R10
R8
TR1
R17
Vref +6V
R3
IC1
R2
G
Input

Fig.2

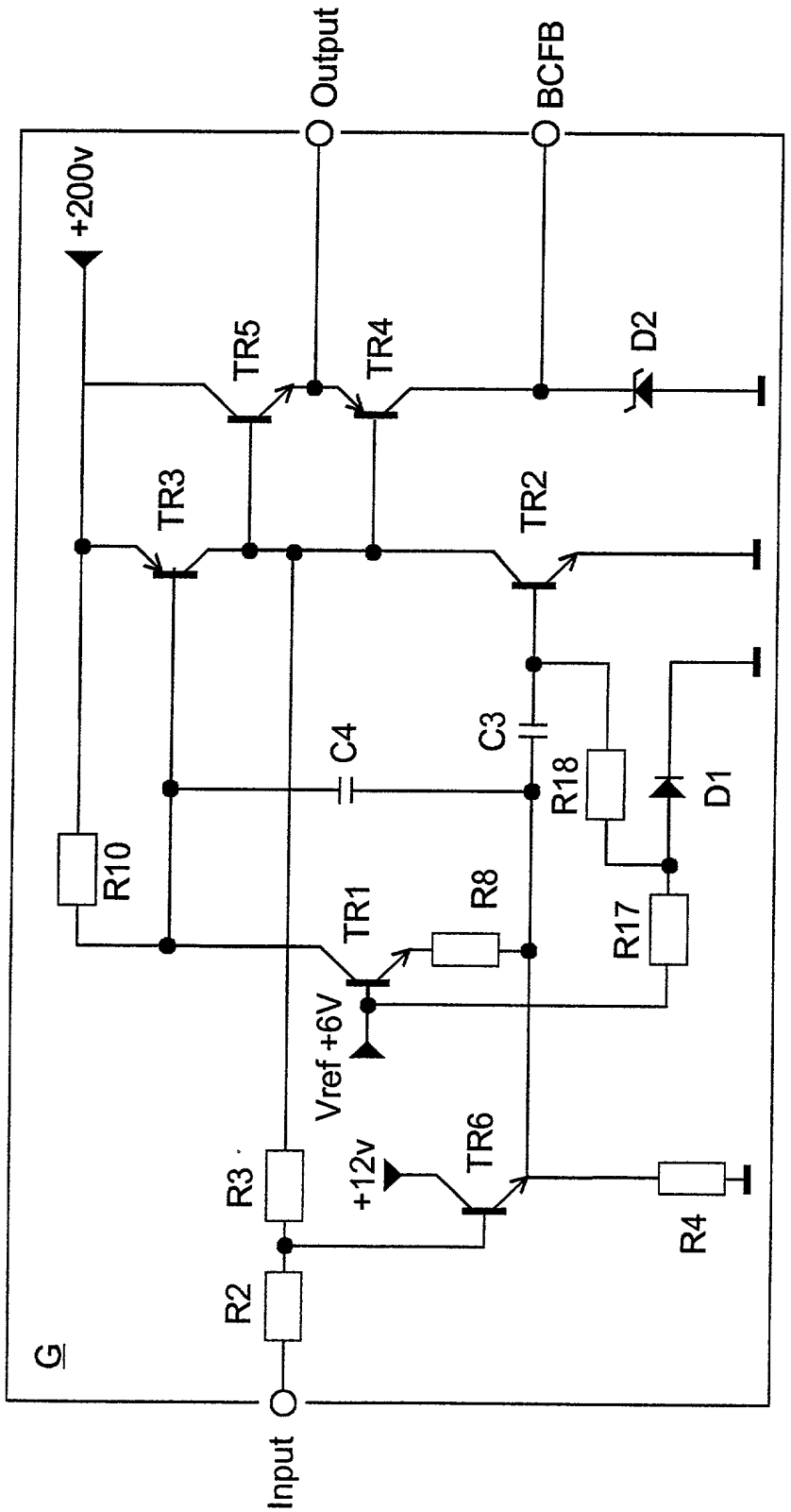
Output
BCFB
+200v
TR5
TR4
D2
TR3
TR2
C4
C3
R18
D1
R10
R8
TR1
R17
Vref +6V
+12v
TR6
R3
R4
R2
G
Input

Fig.3

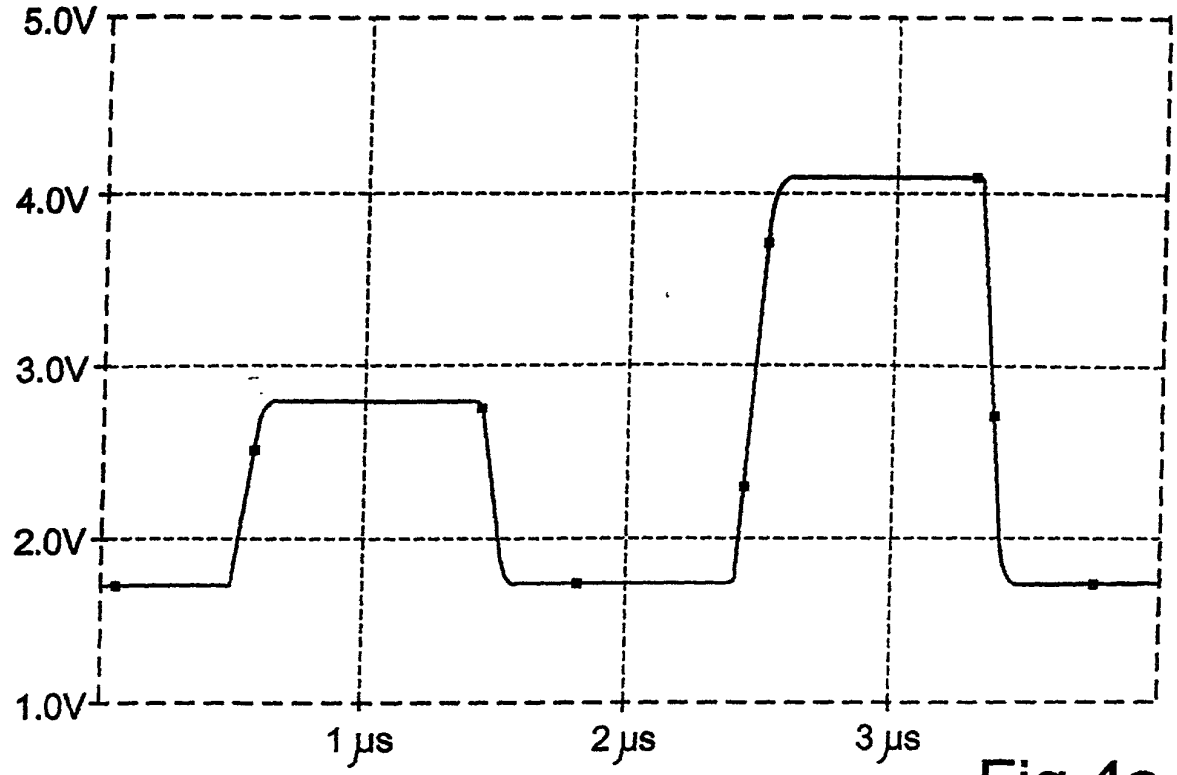

Fig.4a

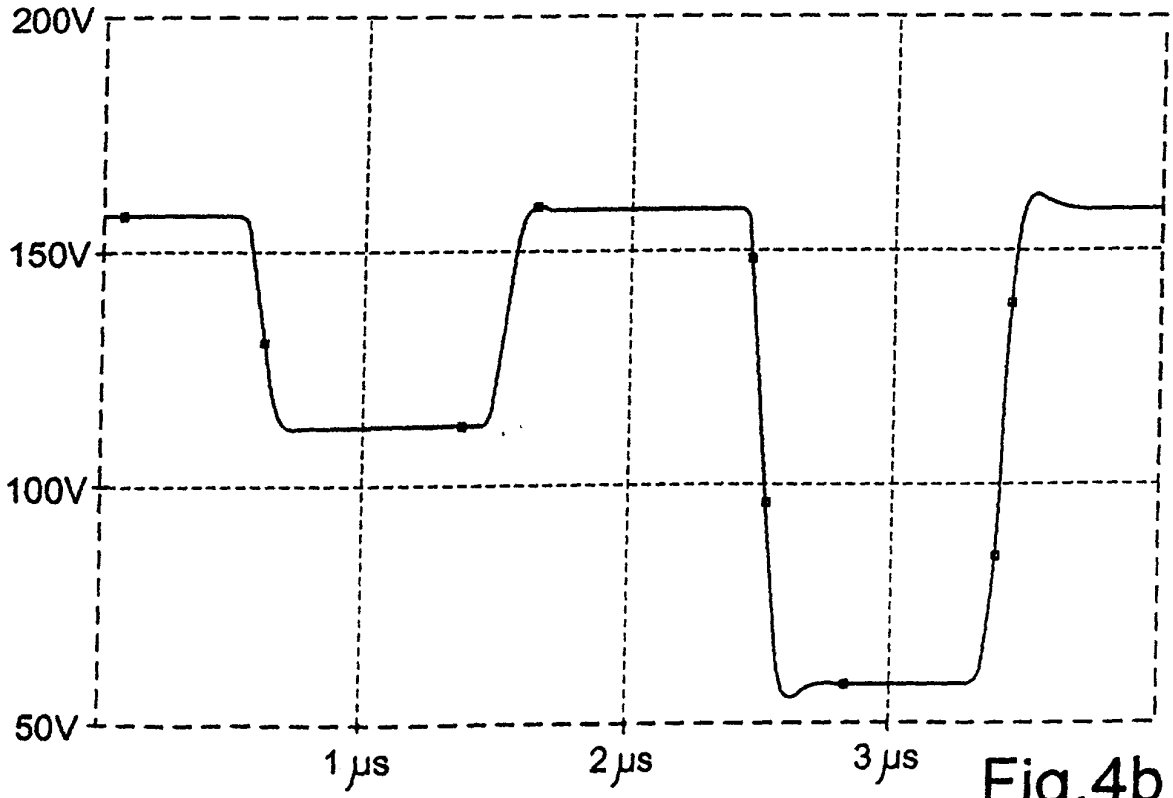

Fig.4b

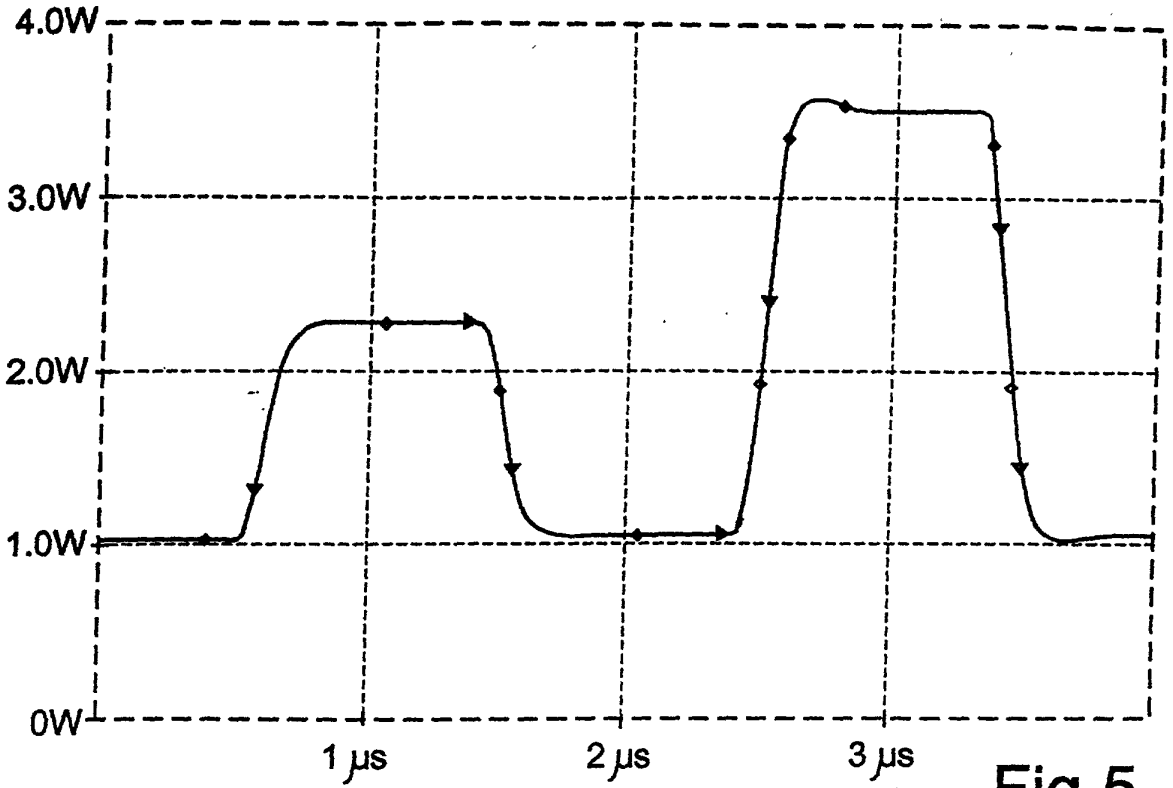

Fig.5

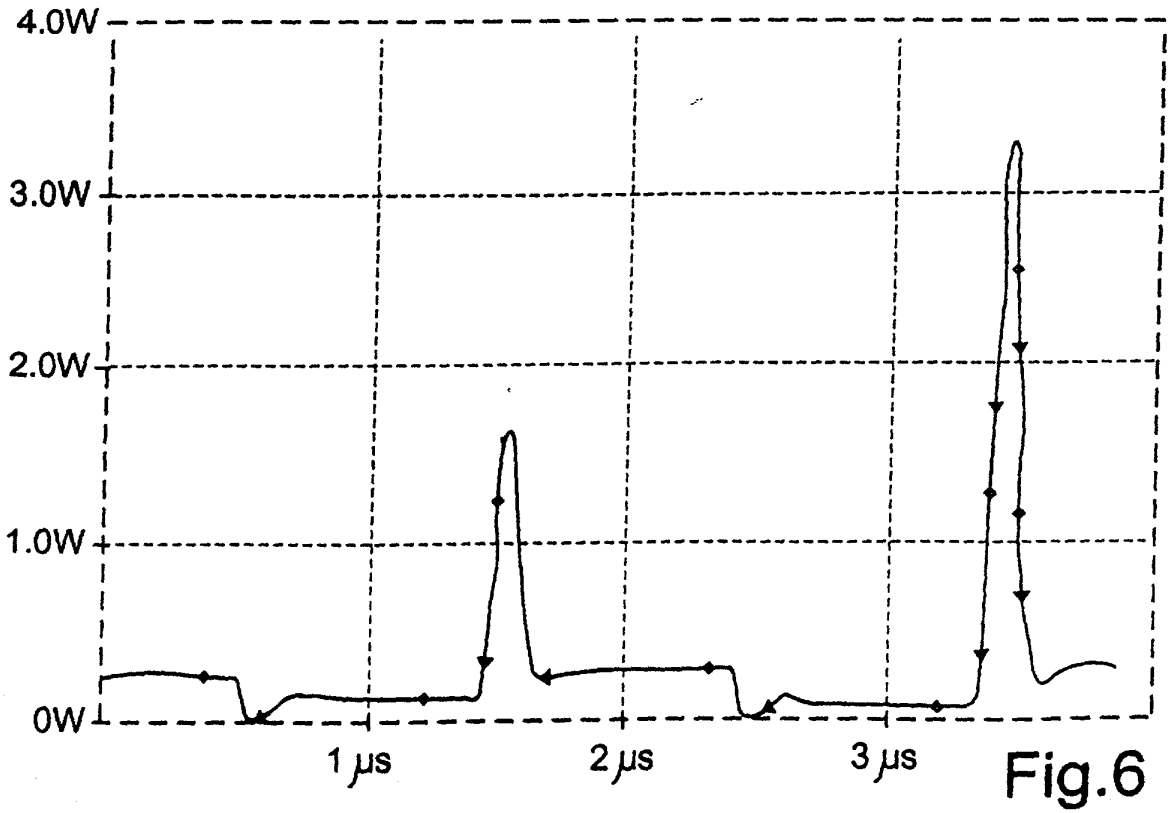

Fig.6

Please type a plus sign (+) inside this box → [+]

PTO/SB/01 (12-97)
Approved for use through 9/30/00. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OBM control number.

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

[X] Declaration Submitted With Initial Filing OR [ ] Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required

Attorney Docket Number	
First Named Inventor	JENSEN, Erik Albert
COMPLETE IF KNOWN	
Application Number	
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A VIDEO OUTPUT AMPLIFIER

(Title of the Invention)

the specification of which

[X] is attached hereto
OR
[ ] was filed on (MM/DD/YYYY) _____ As United States Application Number or PCT International Application Number _____ And was amended on (MM/DD/YYYY) _____ (If applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached YES	Certified Copy Attached No
PA 1998 01371	Denmark	10.23.1998	[ ]	[ ]	[X]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]

[ ] Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	[ ] Additional provisional application Numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

Please type a plus sign (+) inside this box → [+]

PTO/SB/01 (12-97)
Approved for use through 9/30/00. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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DECLARATION - Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number *(if applicable)*

[ ] Additional U.S. or PCT international application numbers are listed on a supplemental priority date sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: [X] Customer Number 22204
OR
[X] Registered practitioner(s) name/registration number listed below.

Name	Registration Number	Name	Registration Number
Daniel W. Sixbey	20,932	Eric J. Robinson	38,285
Stuart J. Friedman	24,312	Frank P. Presta	19,828
Charles M. Leedom, Jr.	26,477	Joseph S. Presta	35,329
Gerald J. Ferguson, Jr.	23,016	Robert M. Schulman	31,196
David S. Safran	27,997	Thomas M Blasey	33,475
Thomas W. Cole	28,290	Daniel S. Song	43,143
Donald R. Studebaker	32,815	Marc S. Kaufman	35,212
Jeffrey L. Costellia	35,483	William J. Healey	36,160
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: [] A petition has been filed for this unsigned inventor.

Given Name (first and middle [if any])	Family Name or Surname
Erik Albert	Jensen

Inventor's Signature: E. A. Jensen Date: April 9. 2001

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[ ] Additional inventors are being named on the _____ Supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.